XEROX
PALO ALTO RESEARCH CENTER
Systems Science Laboratory
LSI Systems Area
October 23, 1978

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To: File

From: Doug Fairbairn

Subject: More NoteTaker I/O information

stored: [IFS] < fairbairn > ntioDev-1.nt

The interrupt controller is addressed as I/O location 0(on the I/O processor) and 800_H on the emulation processor. We will be running this controller in a nested interrupt mode where higher priority devices can interrupt those of lower priority. The processor can mask off any interrupts which are not desired. The highest priority interrupt is level 0 and level 7 is the lowest.

The interrupts are triggered by a postive going edge and they must remain high until the interrupt is serviced.

The controller must be initialized with 3 initialization words. They are as follows:

ICW1 - XXX1 0011 - 13_H IOP address: 0 EP address: 800_H
ICW2 - 0010 0000 - 20_H IOP address:2 EP address: 802_H
ICW3 - not used
ICW4 - 0000 0001 - 1_H IOP address:2 EP address: 802_H

It is important that the control words be output in the order shown.

The mask bit register (a 1 disables an interrupt on that channel) is loaded by writing the mask to address 2_H (IOP) or 802_H (EP). A 1 bit in the LSB of the word masks the highest priority channel.

The "in service" bit for the current interrupt may be reset by writing a 20H to locations 0H (IOP) or 800H (EP).

There is another word which can be written to the device which determines what data comes back on a read. The data to be written is either A_H and B_H. This data is wirtten into location 0_H (IOP) or 800_H (EP). If an A_H is written then subsequent reads of location 0_H or 800_H (EP) will get you the Interrupt Request Register (pending interrupts). If you write a B, subsequent reads will get you the In Service Register (all the interrupts which are currently being serviced). A read of location 2_H or 802_H (EP) will always get you the current mask register.

CRT Controller

The CRT has many internal registers for setting a multitude of internal timing parameters. he folowing data, when loaded into the associated locations should give the proper timinig for the NoteTaker.

Address:	Data:
140H	60H
142H	F0H
144H	7DH
146H	1EH
148H	not used
14AH	Read the line on which the cursor is displayed
14CH	Read Cursor character
14EH	Reset device (stop all timing generation)
150H	Scrolling - not used
152H	Load cursor character address
154H	Load cursor line address
156H	Start timng chain after reset
158H	Self load - not used

The cursor line address is used to stop the generation of any video. It will automatically restart at the beginning of the next field.

The bit clock is settable as well. It is a 36Mhz. osciallator with a programmable divider. The register which holds the timing is at location 100H. It is a 16 bit register of which only 4 of the bits program the bit clock. The whole register is used as follows:

Bits 0-1 (MXXX XXXX XXXX XXXX)- Analog to digital converter speed
- 00 - 3 Khz.
- 01 - 4 Khz.
- 10 - 6 Khz.
- 11 - 12 Khz.

Bit 2 (XXMX XXXX XXXX XXXX)
- 0 -stop the CRT timing chain in its current state
- 1 - allow it to proceed

Bits 3-6 (XXXM MMMX XXXX XXXX) - Bit clock speed
- 0000 - 2.25 Mhz.
- 0001 - 2.4 Mhz
- 0010 - 2.57 Mhz.
- 0011 - 2.76
- 0100 - 3.0 Mhz.
- 0101 - 3.27
- 0110 - 3.6 Mhz.
- 0111 - 4 Mhz
- 1000 - 4.5 Mhz.
- 1001 - 5.14 Mhz.
- 1010 - 6.0 Mhz.
- 1011 - 7.2 Mhz.
- 1100 - 9 Mhz.
- 1101 - 12 Mhz.
- 1110 - 18 Mhz.

Bits 7-9 (XXXX XXXM MMXX XXX) - Select A/D source

- 000 - Tablet X
- 001 - Tablet Y
- 010 - Main +5 volts
- 011 - Main +12 volts(scaled by 1/3)
- 100 - Battery output voltage (scaled by 1/10)
- 101 - External analog 0
- 110 - External analog 1
- 111 - External anlalog 2

Bits 10-12 (XXXX XXXX XXMM MXXX)
Drive select (bit 10=drive 1, bit 11= drive 2, bit 12=drive 3) for the floppy in a multi floppy system. Only one bit may be on at a time.

Bit 13 - (XXXX XXXX XXXX XMXX) - Side select for floppy

Bit 14 - (XXXX XXXX XXXX XXMX) - Turn on 5 volt disk power

Bit 15 - (XXXX XXXX XXXX XXXM) - Turn on 12 volt disk power

NOTE: All bits are set and reset at once. The programmer must keep track of the revious states of bits.